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(54) **SEMICONDUCTOR DEVICE WITH BUMP INTERCONNECTION**

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See application file for complete search history.

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(51) **Int. Cl.**

(57) **ABSTRACT**

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*H01L 23/48* (2006.01)

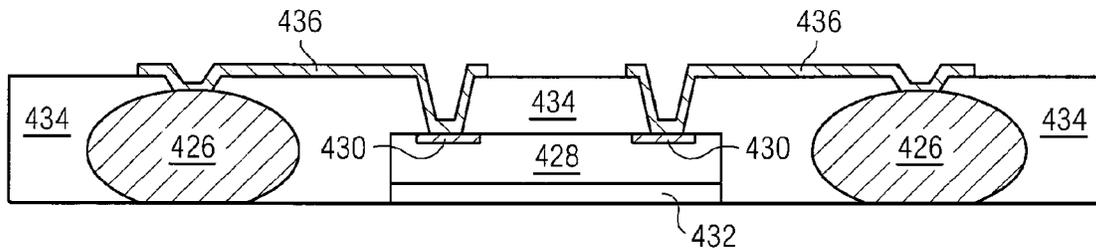
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A semiconductor device includes a semiconductor die having contact pads disposed over a surface of the semiconductor die, a die attach adhesive layer disposed under the semiconductor die, and an encapsulant material disposed around and over the semiconductor die. The semiconductor device further includes bumps disposed in the encapsulant material around a perimeter of the semiconductor die. The bumps are partially enclosed by the encapsulant material. The semiconductor device further comprises first vias disposed in the encapsulant. The first vias expose surfaces of the contact pads. The semiconductor device further includes a first redistribution layer (RDL) disposed over the encapsulant and in the first vias, and a second RDL disposed under the encapsulant material and the die attach adhesive layer. The first RDL electrically connects each contact pad of the semiconductor die to one of the bumps, and the second RDL is electrically connected to one of the bumps.

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**30 Claims, 6 Drawing Sheets**



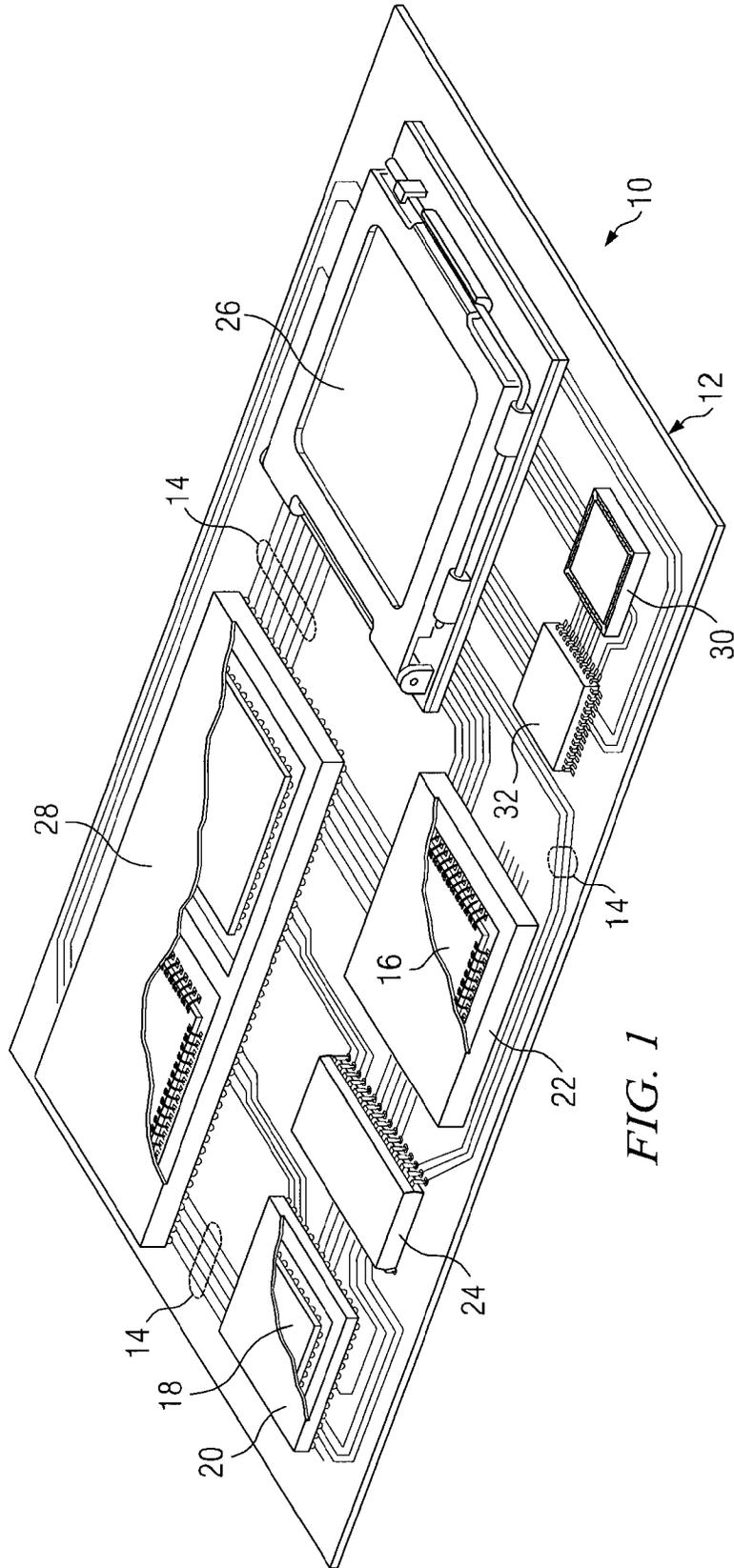
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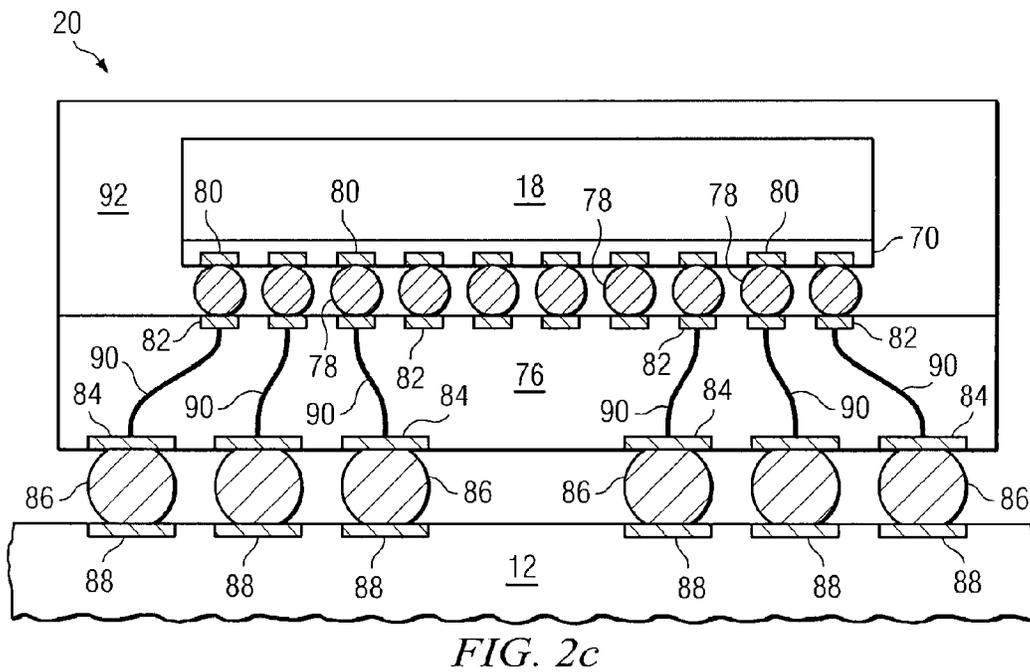
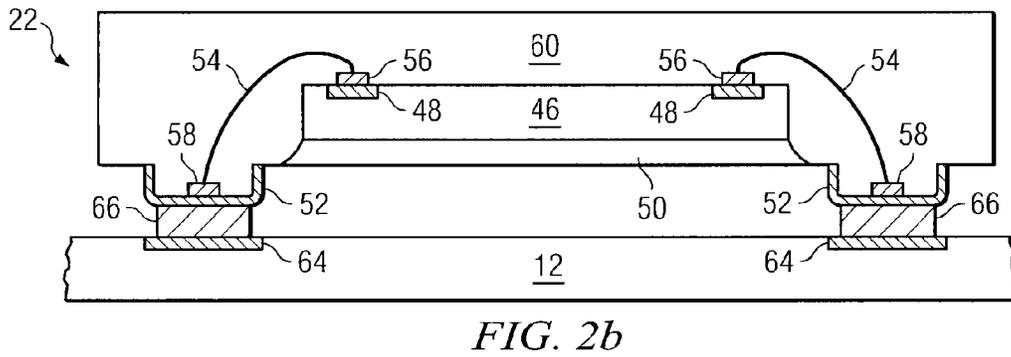
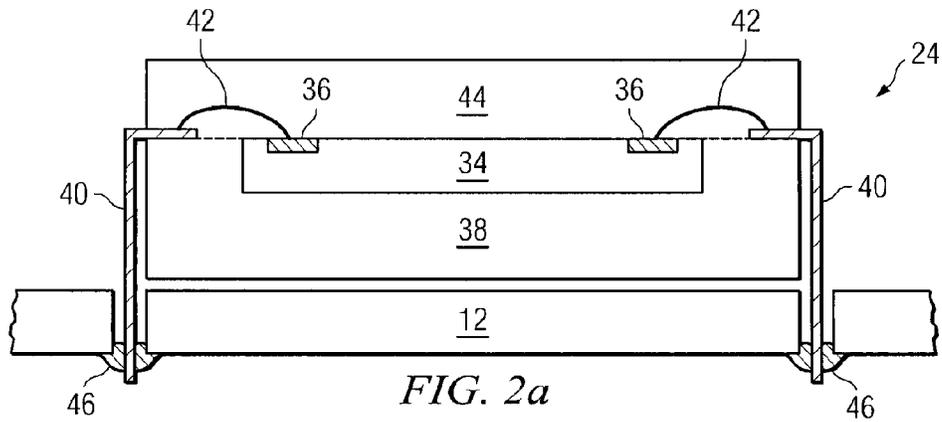
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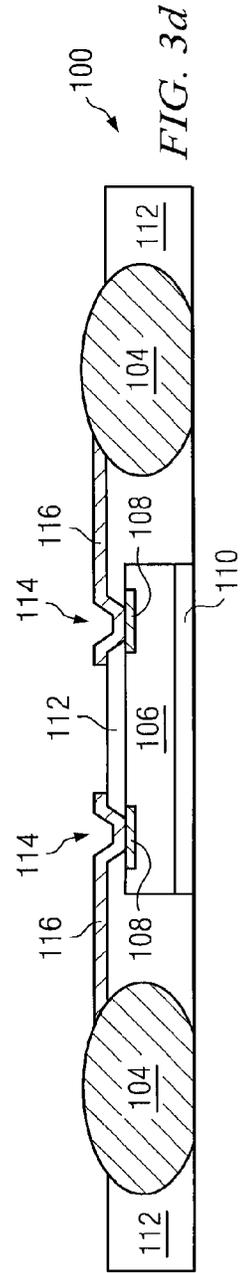
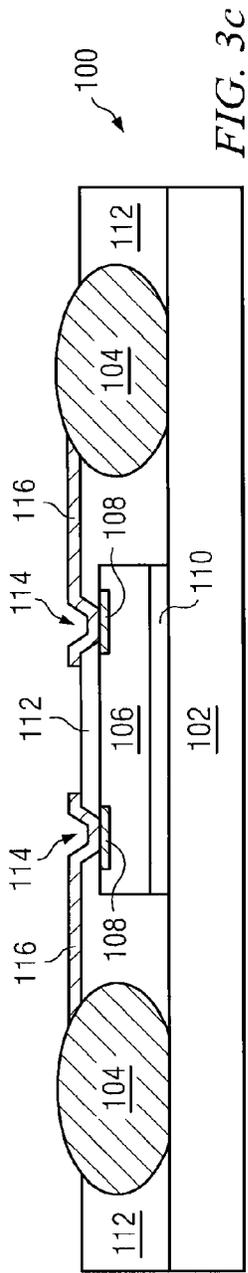
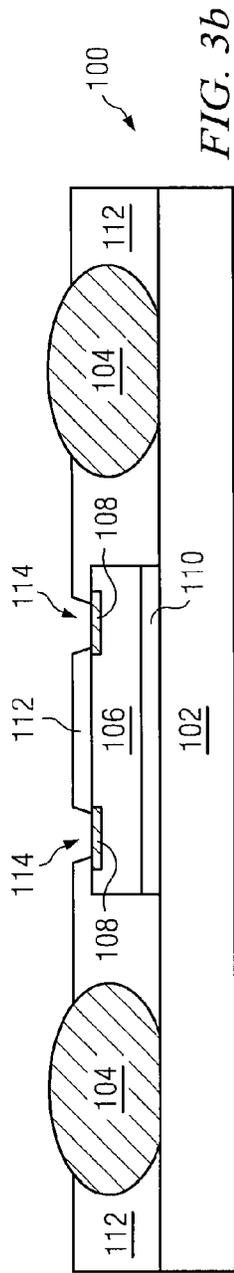
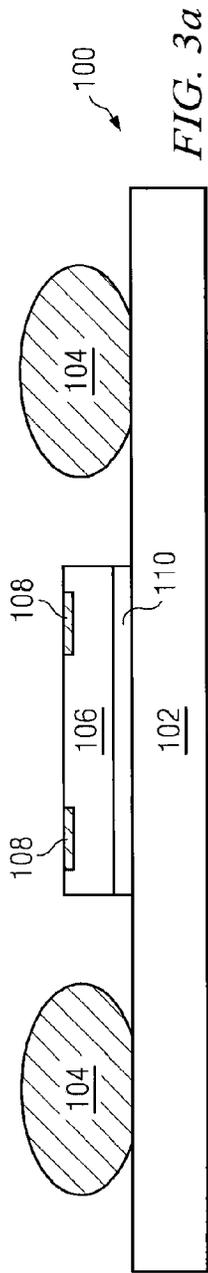
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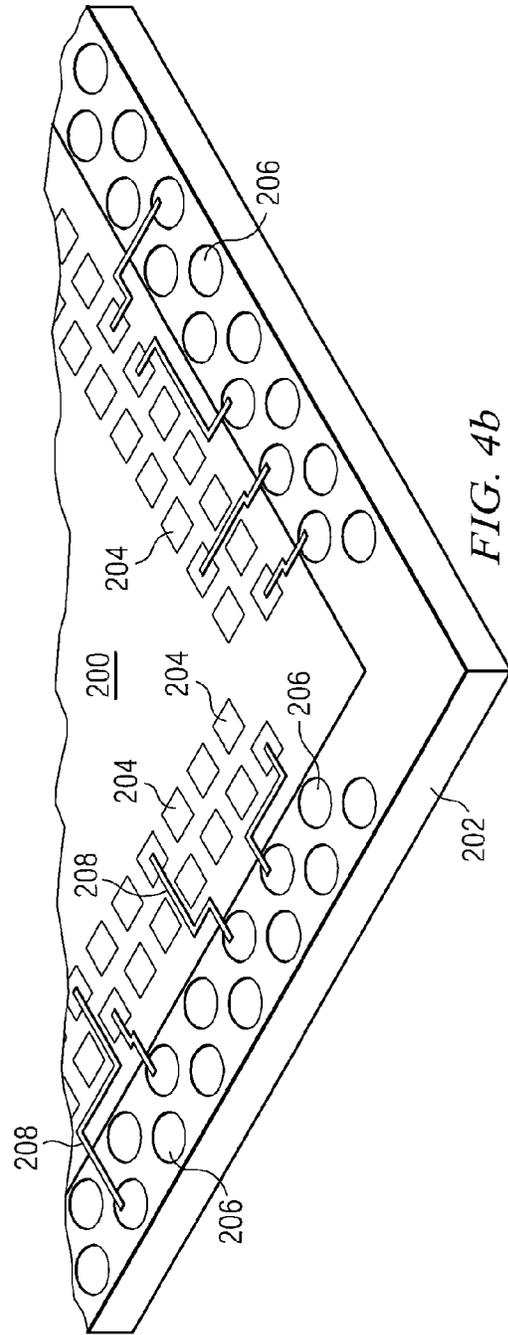
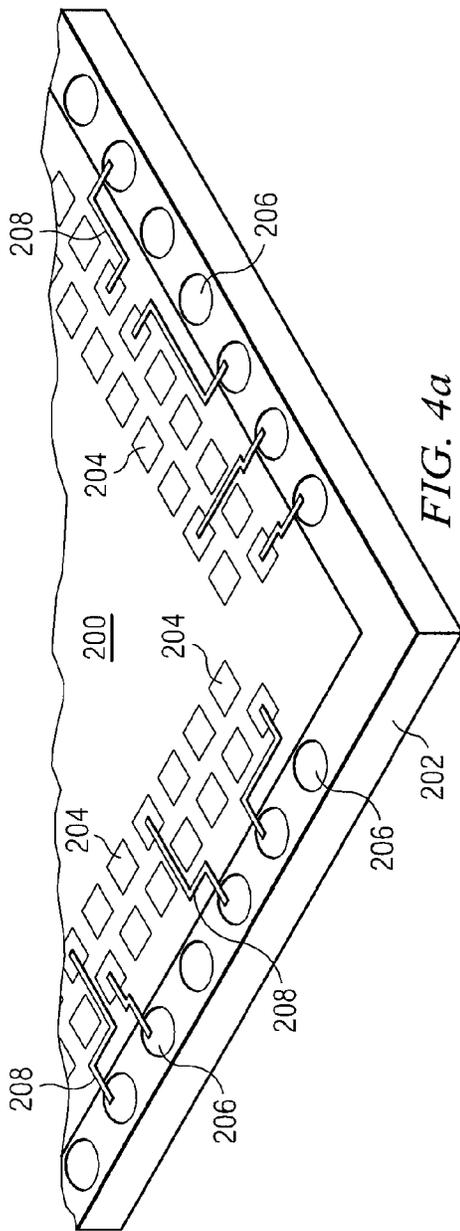
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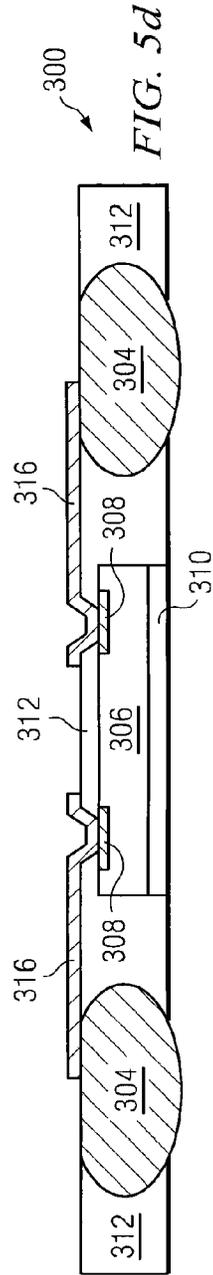
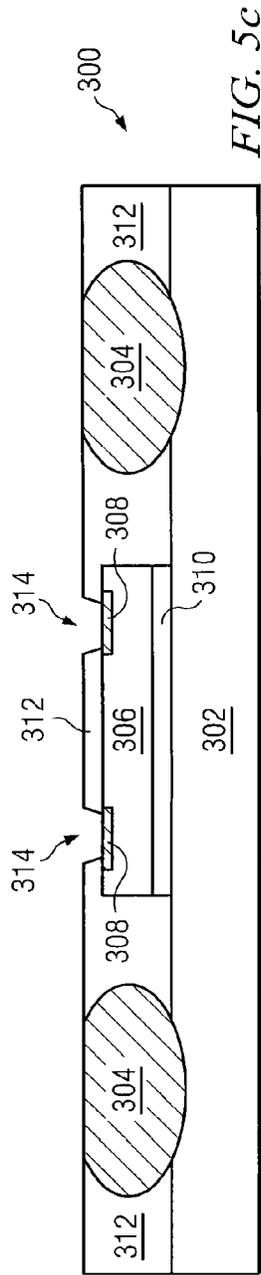
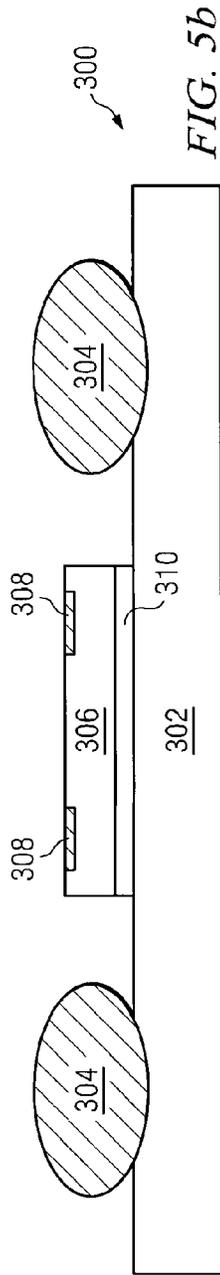
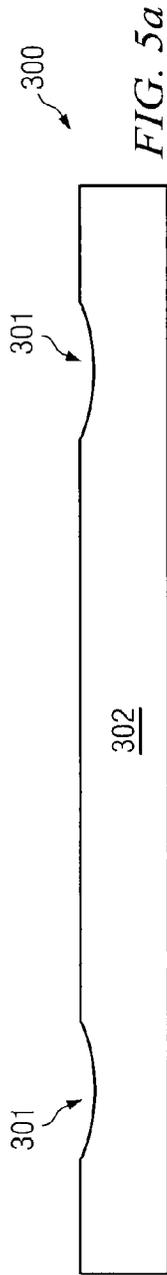
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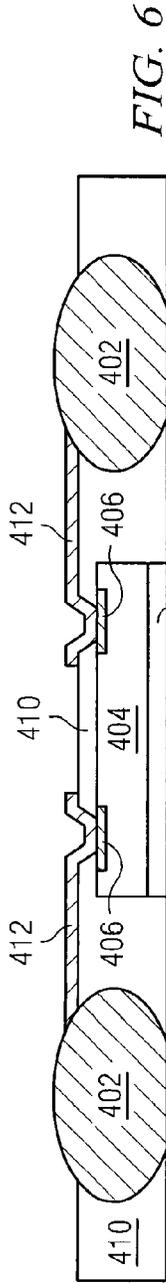


FIG. 6

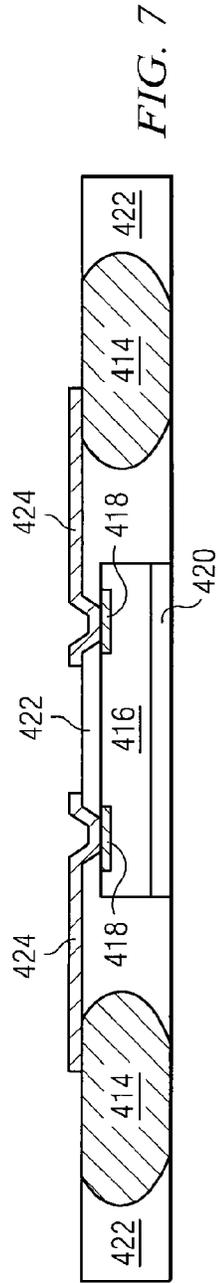


FIG. 7

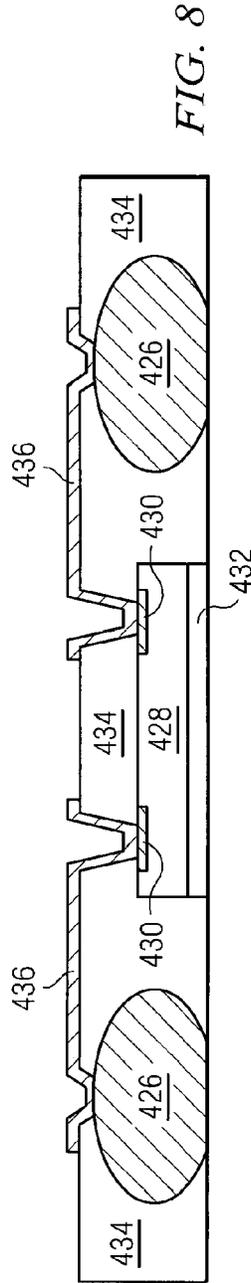


FIG. 8

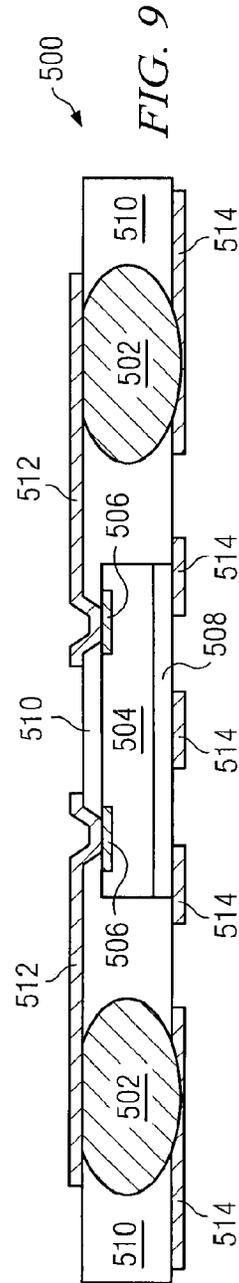


FIG. 9

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## SEMICONDUCTOR DEVICE WITH BUMP INTERCONNECTION

### CLAIM TO DOMESTIC PRIORITY

The present application is a division of U.S. patent application Ser. No. 12/235,000, now U.S. Pat. No. 7,888,181, filed Sep. 22, 2008, and claims priority to the foregoing parent application pursuant to 35 U.S.C. §121.

### FIELD OF THE INVENTION

The present invention relates in general to semiconductor devices and, more particularly, to a semiconductor device including a wafer-level chip-scale package (CSP) having a top and bottom bump interconnect structure.

### BACKGROUND OF THE INVENTION

Semiconductor devices are commonly found in modern electronic products. Semiconductor devices vary in the number and density of electrical components. Discrete semiconductor devices generally contain one type of electrical component, e.g., light emitting diode (LED), transistor, resistor, capacitor, inductor, and power metal oxide semiconductor field effect transistor (MOSFET). Integrated semiconductor devices typically contain hundreds to millions of electrical components. Examples of integrated semiconductor devices include microcontrollers, microprocessors, charged-coupled devices (CCDs), solar cells, and digital micro-mirror devices (DMDs).

Semiconductor devices perform a wide range of functions such as high-speed calculations, transmitting and receiving electromagnetic signals, controlling electronic devices, transforming sunlight to electricity, and creating visual projections for television displays. Semiconductor devices are found in the fields of entertainment, communications, power generation, networks, computers, and consumer products. Semiconductor devices are also found in electronic products including military, aviation, automotive, industrial controllers, and office equipment.

Semiconductor devices exploit the electrical properties of semiconductor materials. The atomic structure of semiconductor material allows its electrical conductivity to be manipulated by the application of an electric field or through the process of doping. Doping introduces impurities into the semiconductor material.

A semiconductor device contains active and passive electrical structures. Active structures, including transistors, control the flow of electrical current. By varying levels of doping and application of an electric field, the transistor either promotes or restricts the flow of electrical current. Passive structures, including resistors, diodes, and inductors, create a relationship between voltage and current necessary to perform a variety of electrical functions. The passive and active structures are electrically connected to form logic circuits, which enable the semiconductor device to perform high-speed calculations and other useful functions.

Semiconductor devices are generally manufactured using two complex manufacturing processes, i.e., front-end manufacturing, and back-end manufacturing, each involving potentially hundreds of steps. Front-end manufacturing involves the formation of a plurality of die on the surface of a semiconductor wafer. Each die is typically identical and contains circuits formed by electrically connecting active and passive components. Back-end manufacturing involves sin-

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gulating individual die from the finished wafer and packaging the die to provide structural support and environmental isolation.

One goal of semiconductor manufacturing is to produce smaller semiconductor devices. Smaller devices typically consume less power, have higher performance, and can be produced more efficiently. In addition, smaller semiconductor devices have a smaller footprint, which is desirable for smaller end products. A smaller die size may be achieved by improvements in the front-end process resulting in die with smaller, higher density active and passive components. Back-end processes may result in semiconductor device packages with a smaller footprint by improvements in electrical interconnection and packaging materials.

Often, when forming wafer-level chip-scale packages (WLCSPs), it is necessary to form top and bottom interconnection structures in the packages. The top and bottom interconnect structure facilitates the mounting of the WLCSPs to motherboards, and other printed circuit boards (PCBs) or substrates. Furthermore, by forming the interconnections on top and bottom surfaces of the package, multiple WLCSPs can be placed over one-another to form stacked packages that provide sophisticated functionality in a small package volume. The top and bottom interconnects usually include conductive through-hole vias (THVs) formed within a perimeter of the WLCSP. Conductive THVs are difficult to manufacture and require several additional fabrication steps that increase the cost and manufacturing time of the WLCSP. Furthermore, as fabrication technologies improve, average die size shrinks and the number of input/output pins per die increases. Due to the increasing pin density, it is difficult to mount the resulting die to conventional motherboards which are configured for ball grid array (BGA) mounting technologies using larger input/output bumps with a larger pitch.

### SUMMARY OF THE INVENTION

In one embodiment, the present invention is a semiconductor device including a semiconductor die having contact pads disposed over a surface of the semiconductor die, a die attach adhesive layer disposed under the semiconductor die, and an encapsulant material disposed around and over the semiconductor die. The semiconductor device further includes bumps disposed in the encapsulant material around a perimeter of the semiconductor die. The bumps are partially enclosed by the encapsulant material. The semiconductor device further comprises first vias disposed in the encapsulant. The first vias expose surfaces of the contact pads. The semiconductor device further includes a first redistribution layer (RDL) disposed over the encapsulant and in the first vias, and a second RDL disposed under the encapsulant material and the die attach adhesive layer. The first RDL electrically connects each contact pad of the semiconductor die to one of the bumps, and the second RDL is electrically connected to one of the bumps.

In another embodiment, the present invention is a semiconductor device including a semiconductor die having a plurality of contact pads disposed over a surface of the semiconductor die, an encapsulant material disposed around the semiconductor die and over the semiconductor die, and a plurality of bumps disposed in the encapsulant material around a perimeter of the semiconductor die. The bumps are partially enclosed by the encapsulant material. The semiconductor device further includes a plurality of first vias disposed in the encapsulant, and a first redistribution layer (RDL) disposed over the encapsulant and in the first vias. The first

vias expose surfaces of the contact pads, and first RDL contacts the surfaces of the contact pads and the bumps.

In still another embodiment, the present invention is a semiconductor device including a semiconductor die having a plurality of contact pads formed over a surface of the semiconductor die, a plurality of bumps disposed around a perimeter of the semiconductor die, and an encapsulant material formed around the bumps and over the semiconductor die. The encapsulant exposes a top portion and a bottom portion of each bump. The semiconductor device further includes a plurality of vias etched into the encapsulant to expose the contact pads of the semiconductor die, and a first redistribution layer (RDL) formed over the encapsulant to connect each contact pad of the semiconductor die to one of the bumps.

In yet another embodiment, the present invention is a semiconductor device including a semiconductor die having a plurality of contact pads, an encapsulant material disposed around the semiconductor die and over the semiconductor die, and a plurality of bumps disposed in the encapsulant material around a perimeter of the semiconductor die. The semiconductor device further includes a plurality of first vias disposed in the encapsulant, and a first redistribution layer (RDL) disposed over the encapsulant and in the first vias. The first vias expose the contact pads, and the first RDL contacts the contact pads and the bumps.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a printed circuit board (PCB) with different types of packages mounted to its surface;

FIGS. 2a-2c illustrate further detail of the representative semiconductor packages mounted to the PCB;

FIGS. 3a-3d illustrate a method of manufacturing a semiconductor device having an interconnect structure providing top and bottom interconnects formed by solder bumps;

FIGS. 4a and 4b illustrate alternative configurations for the plurality of solder bumps that form the interconnect structure of the present semiconductor device;

FIGS. 5a-5d illustrate a method of manufacturing a semiconductor device having an interconnect structure providing top and bottom interconnects formed by solder bumps, the semiconductor device is manufactured using a substrate having solder capture dents;

FIG. 6 illustrates a semiconductor device having an interconnect structure providing top and bottom interconnects formed by solder bumps, a top surface of the solder bumps protrudes past a top-surface of the encapsulant;

FIG. 7 illustrates a semiconductor device having an interconnect structure providing top and bottom interconnects formed by solder bumps, a top surface of the semiconductor device is planarized to expose the solder bumps;

FIG. 8 illustrates a semiconductor device having an interconnect structure providing top and bottom interconnects formed by solder bumps, vias are formed in the encapsulant to expose contact pads of the die and a top surface of the solder bumps; and

FIG. 9 illustrates a semiconductor device having an interconnect structure providing top and bottom interconnects formed by solder bumps, redistribution layers (RDLs) are formed over a top surface and a bottom surface of the semiconductor device.

#### DETAILED DESCRIPTION OF THE DRAWINGS

The present invention is described in one or more embodiments in the following description with reference to the Figures, in which like numerals represent the same or similar

elements. While the invention is described in terms of the best mode for achieving the invention's objectives, it will be appreciated by those skilled in the art that it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims and their equivalents as supported by the following disclosure and drawings.

Semiconductor devices are generally manufactured using two complex manufacturing processes: front-end manufacturing and back-end manufacturing. Front-end manufacturing involves the formation of a plurality of die on the surface of a semiconductor wafer. Each die on the wafer contains active and passive electrical components which are electrically connected to form functional electrical circuits. Active electrical components, such as transistors, have the ability to control the flow of electrical current. Passive electrical components, such as capacitors, inductors, resistors, and transformers, create a relationship between voltage and current necessary to perform electrical circuit functions.

Passive and active components are formed on the surface of the semiconductor wafer by a series of process steps including doping, deposition, photolithography, etching, and planarization. Doping introduces impurities into the semiconductor material by techniques such as ion implantation or thermal diffusion. The doping process modifies the electrical conductivity of semiconductor material in active devices, transforming the semiconductor material into a permanent insulator, permanent conductor, or changing the way the semiconductor material changes in conductivity in response to an electric field. Transistors contain regions of varying types and degrees of doping arranged as necessary to enable the transistor to promote or restrict the flow of electrical current upon the application of an electric field.

Active and passive components are formed by layers of materials with different electrical properties. The layers can be formed by a variety of deposition techniques determined in part by the type of material being deposited. For example, thin film deposition may involve chemical vapor deposition (CVD), physical vapor deposition (PVD), electrolytic plating, and electroless plating processes. Each layer is generally patterned to form portions of active components, passive components, or electrical connections between components.

The layers can be patterned using photolithography, which involves the deposition of light sensitive material, e.g., photoresist, over the layer to be patterned. A pattern is transferred from a photomask to the photoresist using light. The portion of the photoresist pattern subjected to light is removed using a solvent, exposing portions of the underlying layer to be patterned. The remainder of the photoresist is removed, leaving behind a patterned layer. Alternatively, some types of materials are patterned by directly depositing the material into the areas or voids formed by a previous deposition/etch process using techniques such as electrolytic plating.

Depositing a thin film of material over an existing pattern can exaggerate the underlying pattern and create a non-uniformly flat surface. A uniformly flat surface is required to produce smaller and more densely packed active and passive components. Planarization can be used to remove material from the surface of the wafer and produce a uniformly flat surface. Planarization involves polishing the surface of the wafer with a polishing pad. An abrasive material and corrosive chemical are added to the surface of the wafer during polishing. The combined mechanical action of the abrasive and corrosive action of the chemical removes any irregular topography, resulting in a uniformly flat surface.

Back-end manufacturing refers to cutting or singulating the finished wafer into the individual die and then packaging

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the die for structural support and environmental isolation. To singulate the die, the wafer is scored and broken along non-functional regions of the wafer called saw streets or scribes. The wafer is singulated using a laser cutting device or saw blade. After singulation, the individual die are mounted to a package substrate that includes pins or contact pads for interconnection with other system components. Contact pads formed over the semiconductor die are then connected to contact pads within the package. The electrical connections can be made with solder bumps, stud bumps, conductive paste, or wirebonds. An encapsulant or other molding material is deposited over the package to provide physical support and electrical isolation. The finished package is then inserted into an electrical system and the functionality of the semiconductor device is made available to the other system components.

FIG. 1 illustrates electronic device 10 having a chip carrier substrate or printed circuit board (PCB) 12 with a plurality of semiconductor packages mounted on its surface. Electronic device 10 may have one type of semiconductor package, or multiple types of semiconductor packages, depending on the application. The different types of semiconductor packages are shown in FIG. 1 for purposes of illustration.

Electronic device 10 may be a stand-alone system that uses the semiconductor packages to perform an electrical function. Alternatively, electronic device 10 may be a subcomponent of a larger system. For example, electronic device 10 may be a graphics card, network interface card, or other signal processing card that can be inserted into a computer. The semiconductor package can include microprocessors, memories, application specific integrated circuits (ASICs), logic circuits, analog circuits, RF circuits, discrete devices, or other semiconductor die or electrical components.

In FIG. 1, PCB 12 provides a general substrate for structural support and electrical interconnect of the semiconductor packages mounted on the PCB. Conductive signal traces 14 are formed on a surface or within layers of PCB 12 using evaporation, electrolytic plating, electroless plating, screen printing, PVD, or other suitable metal deposition process. Signal traces 14 provide for electrical communication between each of the semiconductor packages, mounted components, and other external system components. Traces 14 also provide power and ground connections to each of the semiconductor packages.

In some embodiments, a semiconductor device has two packaging levels. First level packaging is the technique for mechanically and electrically attaching the semiconductor die to a carrier. Second level packaging involves mechanically and electrically attaching the carrier to the PCB. In other embodiments, a semiconductor device may only have the first level packaging where the die is mechanically and electrically mounted directly to the PCB.

For the purpose of illustration, several types of first level packaging, including wire bond package 16 and flip chip 18, are shown on PCB 12. Additionally, several types of second level packaging, including ball grid array (BGA) 20, bump chip carrier (BCC) 22, dual in-line package (DIP) 24, land grid array (LGA) 26, multi-chip module (MCM) 28, quad flat non-leaded package (QFN) 30, and quad flat package 32, are shown mounted on PCB 12. Depending upon the system requirements, any combination of semiconductor packages, configured with any combination of first and second level packaging styles, as well as other electronic components, can be connected to PCB 12. In some embodiments, electronic device 10 includes a single attached semiconductor package, while other embodiments call for multiple interconnected packages. By combining one or more semiconductor pack-

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ages over a single substrate, manufacturers can incorporate pre-made components into electronic devices and systems. Because the semiconductor packages include sophisticated functionality, electronic devices can be manufactured using cheaper components and a shorter manufacturing process. The resulting devices are less likely to fail and less expensive to manufacture resulting in lower costs for consumers.

FIG. 2a illustrates further detail of DIP 24 mounted on PCB 12. DIP 24 includes semiconductor die 34 having contact pads 36. Semiconductor die 34 includes an active area containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within semiconductor die 34 and are electrically interconnected according to the electrical design of the die. For example, the circuit may include one or more transistors, diodes, inductors, capacitors, resistors, and other circuit elements formed within the active area of die 34. Contact pads 36 are made with a conductive material, such as aluminum (Al), copper (Cu), tin (Sn), nickel (Ni), gold (Au), or silver (Ag), and are electrically connected to the circuit elements formed within die 34. Contact pads 36 are formed by PVD, CVD, electrolytic plating, or electroless plating process. During assembly of DIP 24, semiconductor die 34 is mounted to a carrier 38 using a gold-silicon eutectic layer or adhesive material such as thermal epoxy. The package body includes an insulative packaging material such as plastic or ceramic. Conductor leads 40 are connected to carrier 38 and wire bonds 42 are formed between leads 40 and contact pads 36 of die 34 as a first level packaging. Encapsulant 44 is deposited over the package for environmental protection by preventing moisture and particles from entering the package and contaminating die 34, contact pads 36, or wire bonds 42. DIP 24 is connected to PCB 12 by inserting leads 40 into holes formed through PCB 12. Solder material 46 is flowed around leads 40 and into the holes to physically and electrically connect DIP 24 to PCB 12. Solder material 46 can be any metal or electrically conductive material, e.g., Sn, lead (Pb), Au, Ag, Cu, zinc (Zn), bismuthinite (Bi), and alloys thereof, with an optional flux material. For example, the solder material can be eutectic Sn/Pb, high-lead, or lead-free.

FIG. 2b illustrates further detail of BCC 22 mounted on PCB 12. Semiconductor die 47 is connected to a carrier by wire bond style first level packaging. BCC 22 is mounted to PCB 12 with a BCC style second level packaging. Semiconductor die 47 having contact pads 48 is mounted over a carrier using an underfill or epoxy-resin adhesive material 50. Semiconductor die 47 includes an active area containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within semiconductor die 47 and are electrically interconnected according to the electrical design of the die. For example, the circuit may include one or more transistors, diodes, inductors, capacitors, resistors, and other circuit elements formed within the active area of die 47. Contact pads 48 are made with a conductive material, such as Al, Cu, Sn, Ni, Au, or Ag, and are electrically connected to the circuit elements formed within die 47. Contact pads 48 are formed by PVD, CVD, electrolytic plating, or electroless plating process. Wire bonds 54 and bond pads 56 and 58 electrically connect contact pads 48 of semiconductor die 47 to contact pads 52 of BCC 22 forming the first level packaging. Molding compound or encapsulant 60 is deposited over semiconductor die 47, wire bonds 54, contact pads 48, and contact pads 52 to provide physical support and electrical isolation for the device. Contact pads 64 are formed on a surface of PCB 12 using evaporation, electrolytic plating, electroless plating, screen printing, PVD, or other suitable metal deposition pro-

cess and are typically plated to prevent oxidation. Contact pads **64** electrically connect to one or more conductive signal traces **14**. Solder material is deposited between contact pads **52** of BCC **22** and contact pads **64** of PCB **12**. The solder material is reflowed to form bumps **66** which form a mechanical and electrical connection between BCC **22** and PCB **12**.

In FIG. **2c**, semiconductor die **18** is mounted face down to carrier **76** with a flip chip style first level packaging. BGA **20** is attached to PCB **12** with a BGA style second level packaging. Active area **70** containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within semiconductor die **18** is electrically interconnected according to the electrical design of the die. For example, the circuit may include one or more transistors, diodes, inductors, capacitors, resistors, and other circuit elements formed within active area **70** of semiconductor die **18**. Semiconductor die **18** is electrically and mechanically attached to the carrier **76** through a large number of individual conductive solder bumps or balls **78**. Solder bumps **78** are formed on bump pads or interconnect sites **80**, which are disposed on active areas **70**. Bump pads **80** are made with a conductive material, such as Al, Cu, Sn, Ni, Au, or Ag, and are electrically connected to the circuit elements formed in active area **70**. Bump pads **80** are formed by PVD, CVD, electrolytic plating, or electroless plating process. Solder bumps **78** are electrically and mechanically connected to contact pads or interconnect sites **82** on carrier **76** by a solder reflow process.

BGA **20** is electrically and mechanically attached to PCB **12** by a large number of individual conductive solder bumps or balls **86**. The solder bumps are formed on bump pads or interconnect sites **84**. The bump pads **84** are electrically connected to interconnect sites **82** through conductive lines **90** routed through carrier **76**. Contact pads **88** are formed on a surface of PCB **12** using evaporation, electrolytic plating, electroless plating, screen printing, PVD, or other suitable metal deposition process and are typically plated to prevent oxidation. Contact pads **88** electrically connect to one or more conductive signal traces **14**. The solder bumps **86** are electrically and mechanically connected to contact pads or bonding pads **88** on PCB **12** by a solder reflow process. Molding compound or encapsulant **92** is deposited over semiconductor die **18** and carrier **76** to provide physical support and electrical isolation for the device. The flip chip semiconductor device provides a short electrical conduction path from the active devices on semiconductor die **18** to conduction tracks on PCB **12** in order to reduce signal propagation distance, lower capacitance, and achieve overall better circuit performance. In another embodiment, the semiconductor die **18** can be mechanically and electrically attached directly to PCB **12** using flip chip style first level packaging without carrier **76**.

FIGS. **3a-3d** illustrate a method of manufacturing semiconductor device **100** having an interconnect structure providing top and bottom interconnects formed by solder bumps. Turning to FIG. **3a**, substrate **102** is provided. In one embodiment, substrate **102** includes a bare Cu sheet suitable for attaching a plurality of solder bumps. In alternative embodiments, substrate **102** includes other metals or substrate materials over which solder bumps may be deposited and connected. A solder material is deposited over substrate **102** using a ball drop or stencil printing process, for example. The solder material includes an electrically conductive material such as Sn, Pb, Au, Ag, Cu, Zn, Bi, and alloys thereof, with an optional flux material. For example, the solder material can be eutectic Sn/Pb, high lead, or lead free. The solder (or other conductive material) is reflowed to form bumps **104**. Bumps **104** are mechanically connected to substrate **102**.

Die **106** is mounted to substrate **102** using die attach adhesive **110**. Die **106** includes semiconductor devices, or other electronic chips or ICs and provides various functions such as memory, controller, ASICs, processor, microcontroller, or combinations thereof. Die attach adhesive **110** includes an underfill or epoxy polymer material for bonding die **106** to substrate **102**. In alternative embodiments, die attach adhesive **110** includes a laminated polymer adhesive or an ultraviolet (UV) curable liquid adhesive, for example. Contact pads **108** are made with a conductive material, such as Al, Cu, Sn, Ni, Au, or Ag, and are electrically connected to the circuit elements formed within die **106**. Contact pads **108** are formed by PVD, CVD, electrolytic plating, or electroless plating processes, for example.

Turning to FIG. **3b**, encapsulant **112** is deposited over substrate **102** around bumps **104** and over die **106**. Encapsulant **112** includes an epoxy resin, or polyimide, for example, and may be deposited by spin-coating, dispensing, or printing. As shown in FIG. **3b**, the deposition of encapsulant **112** is controlled to expose a top surface of bumps **104**. Depending upon the application, 1-25% of the surface of bumps **104** are exposed above the encapsulant **112**. In an alternative embodiment, the exposed portions of bumps **104** are flattened after deposition of encapsulant **112** to be level with a top surface of encapsulant **112**. Vias **114** are formed in encapsulant **112** by blind etching to expose contact pads **108**. Blind etching involves removing a portion of encapsulant **112** and may be performed by laser drilling or etching, wet etching, or another etching process.

Turning to FIG. **3c**, redistribution layer (RDL) **116** is deposited over semiconductor device **100** to interconnect bumps **104** and contact pads **108** of die **106**. RDL **116** can be made with Ni, NiV, Cu, or other conductive materials. RDL **116** routes electrical signals between die **106** and bumps **104**. RDL **116** is formed by PVD, CVD, electrolytic plating, or electroless plating processes. With RDL **116** deposited, bumps **104** are electrically connected to the circuits and devices formed within die **106**.

Turning to FIG. **3d**, a backgrinding process is applied to substrate **102** to remove substrate **102** and to expose a back surface of bumps **104** and die attach adhesive **110**. The backgrinding process may involve chemical-mechanical polishing (CMP), wet etching, plasma etching, or another etching process suitable for removing substrate **102**. With substrate **102** removed, semiconductor device **100** may be mounted to motherboards, PCBs, or other substrates using bumps **104** as the interconnect structure for placing die **106** in communication with other system components. An optional passivation layer (not shown) is deposited over semiconductor device **100** to cover RDL **116** and provide electrical insulation and physical protection. The optional passivation layer may include one or more layers of silicon dioxide (SiO<sub>2</sub>), silicon nitride (Si<sub>3</sub>N<sub>4</sub>), silicon oxy-nitride (SiON), or another insulating material.

Using the above method, a semiconductor device is formed that provides a wafer-level chip-scale package (WL CSP) having both top and bottom surface interconnects. Rather than use through-silicon or through-hole vias, which require an expensive and time-consuming manufacturing process, the interconnect structure is formed by a plurality of solder bumps. The bumps are formed using a simplified manufacturing process that allows for formation of the bumps directly over a copper strip, or other metal substrate. Because the bumps are formed directly on the substrate, additional pad layers for building up the bumps or insulation layers are not necessary.

An encapsulant is deposited over the device and a top and bottom surface of the solder bumps are exposed to provide top and bottom surface interconnects for the semiconductor device. An RDL structure is formed over the device to interconnect the bumps and the die. In the present embodiment, the RDL structure is flat and formed directly over a surface of the encapsulant. Because the interconnect structure of the semiconductor device is formed by solder bumps rather than small input/output pins, the process of mounting the device to a motherboard configured for BGA-type device mounting is simplified. Accordingly, the present method mitigates several difficulties associated with forming WLCSPs using dies having relatively high input/output pin counts.

FIGS. 4a and 4b illustrate alternative configurations for the plurality of solder bumps that form the interconnect structure of the present semiconductor device. Turning to FIG. 4a, a plurality of solder bumps 206 are disposed within encapsulant 202 deposited around die 200. The deposition of encapsulant 202 is controlled to expose a top surface of bumps 206 and contact pads 204 that are formed over a surface of die 200. RDL 208 is formed over a surface of encapsulant 202 and die 200 to form an electrical interconnection between die 200 and bumps 206. As shown in FIG. 4a, bumps 206 provide a single row of interconnect structures to facilitate mounting the device to other system components. In alternative embodiments, bumps 206 are configured in multiple rows. As shown in FIG. 4b, bumps 206 are configured in two rows of staggered bumps 206. RDL 208 is deposited over die 200 and encapsulant 202 to connect bumps 206 from both rows to contact pads 204 of die 200.

FIGS. 5a-5d illustrate a method of manufacturing semiconductor device 300 having an interconnect structure providing top and bottom interconnects formed by solder bumps, semiconductor device 300 is manufactured using a substrate having solder capture dents 301. Turning to FIG. 5a, substrate 302 is provided. In one embodiment, substrate 302 includes a bare Cu sheet suitable for attaching a plurality of solder bumps. Solder capture dents 301 are formed within a surface of substrate 302 to facilitate the deposition of conductive material over substrate 302. In one embodiment, solder capture dents 301 are configured to receive 1-25% of the total volume of bumps 304. Generally, the geometric shape of solder capture dents 301 is semi-spherical, however other configurations may be used depending upon the application.

Turning to FIG. 5b, a solder material is deposited over solder capture dents 301 of substrate 302 using a ball drop or stencil printing process, for example. The solder material includes an electrically conductive material such as Sn, Pb, Au, Ag, Cu, Zn, Bi, and alloys thereof, with an optional flux material. The solder (or other conductive material) is reflowed to form bumps 304. Bumps 304 are mechanically connected to substrate 302.

Die 306 is mounted to substrate 302 using die attach adhesive 310. Die 306 includes semiconductor devices, or other electronic chips or ICs and provides various functions such as memory, controller, ASICs, processor, microcontroller, or combinations thereof. Die attach adhesive 310 includes an underfill or epoxy polymer material for bonding die 306 to substrate 302. In alternative embodiments, die attach adhesive 310 includes a laminated polymer adhesive or an UV curable liquid adhesive, for example. Contact pads 308 are made with a conductive material, such as Al, Cu, Sn, Ni, Au, or Ag, and are electrically connected to the circuit elements formed within die 306. Contact pads 308 are formed by PVD, CVD, electrolytic plating, or electroless plating processes, for example.

Turning to FIG. 5c, encapsulant 312 is deposited over substrate 302 around bumps 304 and over die 306. Encapsulant 312 includes an epoxy resin, or polyimide, for example, and may be deposited by spin-coating, dispensing, printing, or transfer molding. As shown in FIG. 5c, the deposition of encapsulant 312 is controlled to expose a top surface of bumps 304, or encapsulant 312 may be planarized to expose bumps 304. Vias 314 are formed in encapsulant 312 by blind etching to expose contact pads 308. Blind etching involves removing a portion of encapsulant 312 and may be performed by laser drilling or etching, wet etching, or another etching process.

Turning to FIG. 5d, RDL 316 is deposited over semiconductor device 300 to interconnect bumps 304 and contact pads 308 of die 306. RDL 316 can be made with Ni, NiV, Cu, or other conductive materials. RDL 316 routes electrical signals between die 306 and bumps 304. RDL 316 is formed by PVD, CVD, electrolytic plating, or electroless plating processes. With RDL 316 deposited, bumps 304 are electrically connected to the circuits and devices formed within die 306.

A backgrinding process is applied to substrate 302 to remove substrate 302 and to expose a back surface of bumps 304 and die attach adhesive 310. The backgrinding process may involve CMP, wet etching, plasma etching, or another etching process suitable for removing substrate 302. With substrate 302 removed, semiconductor device 300 may be mounted to motherboards, PCBs, or other substrates using bumps 304 as the interconnect structure for placing die 306 in communication with other system components. An optional passivation layer (not shown) is deposited over semiconductor device 300 to cover RDL 316 and provide electrical insulation and physical protection. The optional passivation layer may include one or more layers of SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, SiON, or another insulating material.

FIG. 6 illustrates a semiconductor device having an interconnect structure providing top and bottom interconnects formed by solder bumps, a top surface of the solder bumps protrudes past a top-surface of the encapsulant. Solder bumps 402 are formed using a ball drop or stencil printing process. Solder material is reflowed to form solder bumps 402. Die 404 is mounted next to bumps 402 using die attach adhesive 408. Die 404 includes semiconductor devices, or other electronic chips or ICs and provides various functions such as memory, controller, ASICs, processor, microcontroller, or combinations thereof. Die attach adhesive 408 includes an underfill or epoxy polymer material. Contact pads 406 are made with a conductive material, such as Al, Cu, Sn, Ni, Au, or Ag, and are electrically connected to the circuit elements formed within die 404. Contact pads 406 are formed by PVD, CVD, electrolytic plating, or electroless plating processes, for example.

Encapsulant 410 is deposited around bumps 402 and over die 404. Encapsulant 410 includes an epoxy resin, or polyimide, for example, and may be deposited by spin-coating, dispensing, or printing. As shown in FIG. 6, the deposition of encapsulant 410 is controlled to expose a top surface of bumps 402. Vias are formed in encapsulant 410 by blind etching to expose contact pads 408.

RDL 412 is deposited over encapsulant 410 to interconnect bumps 402 and contact pads 406 of die 404. RDL 412 can be made with Ni, NiV, Cu, or other conductive materials. RDL 412 routes electrical signals between die 404 and bumps 402. RDL 412 is formed by PVD, CVD, electrolytic plating, or electroless plating processes. With RDL 412 deposited, bumps 402 are electrically connected to the circuits and devices formed within die 404.

An optional passivation layer (not shown) is deposited over the semiconductor device to cover RDL **412** and provide electrical insulation and physical protection. The optional passivation layer may include one or more layers of SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, SiON, or another insulating material.

FIG. 7 illustrates a semiconductor device having an interconnect structure providing top and bottom interconnects formed by solder bumps, a top surface of the semiconductor device is planarized to expose the solder bumps. Solder bumps **414** are formed using a ball drop or stencil printing process. Solder material is reflowed to form solder bumps **414**. Die **416** is mounted next to bumps **414** using die attach adhesive **420**. Die **416** includes semiconductor devices, or other electronic chips or ICs and provides various functions such as memory, controller, ASICs, processor, microcontroller, or combinations thereof. Die attach adhesive **420** includes an underfill or epoxy polymer material. Contact pads **418** are made with a conductive material, such as Al, Cu, Sn, Ni, Au, or Ag, and are electrically connected to the circuit elements formed within die **416**. Contact pads **418** are formed by PVD, CVD, electrolytic plating, or electroless plating processes, for example.

Encapsulant **422** is deposited over bumps **414** and over die **416**. Encapsulant **422** includes an epoxy resin, or polyimide, for example, and may be deposited by spin-coating, dispensing, or printing. After encapsulant **422** is deposited, it is planarized to remove a portion of encapsulant **422** and to expose a top surface of bumps **414**. During planarization, a portion of both encapsulant **422** and bumps **424** may be removed. Encapsulant **422** is planarized using a CMP, mechanical backgrinding, plasma etching, wet etch, dry etch or other thinning or planarization process. Vias are formed in encapsulant **422** by blind etching to expose contact pads **418**.

RDL **424** is deposited over encapsulant **422** to interconnect bumps **414** and contact pads **418** of die **416**. RDL **424** can be made with Ni, NiV, Cu, or other conductive materials. RDL **424** routes electrical signals between die **416** and bumps **414**. RDL **424** is formed by PVD, CVD, electrolytic plating, or electroless plating processes. With RDL **424** deposited, bumps **414** are electrically connected to the circuits and devices formed within die **416**.

An optional passivation layer (not shown) is deposited over the semiconductor device to cover RDL **424** and provide electrical insulation and physical protection. The optional passivation layer may include one or more layers of SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, SiON, or another insulating material.

FIG. 8 illustrates a semiconductor device having an interconnect structure providing top and bottom interconnects formed by solder bumps, vias are formed in the encapsulant to expose contact pads of the die and a top surface of the solder bumps. Solder bumps **426** are formed using a ball drop or stencil printing process. Solder material is reflowed to form solder bumps **426**. Die **428** is mounted next to bumps **426** using die attach adhesive **432**. Die **428** includes semiconductor devices, or other electronic chips or ICs and provides various functions such as memory, controller, ASICs, processor, microcontroller, or combinations thereof. Die attach adhesive **432** includes an underfill or epoxy polymer material. Contact pads **430** are made with a conductive material, such as Al, Cu, Sn, Ni, Au, or Ag, and are electrically connected to the circuit elements formed within die **428**. Contact pads **430** are formed by PVD, CVD, electrolytic plating, or electroless plating processes, for example.

Encapsulant **434** is deposited over bumps **426** and over die **428**. Encapsulant **434** includes an epoxy resin, or polyimide, for example, and may be deposited by spin-coating, dispens-

ing, or printing. Vias are formed in encapsulant **434** by blind etching to expose both contact pads **430** and a top surface of bumps **426**.

RDL **436** is deposited over encapsulant **434** to interconnect bumps **426** and contact pads **430** of die **428**. RDL **436** can be made with Ni, NiV, Cu, or other conductive materials. RDL **436** routes electrical signals between die **428** and bumps **426**. RDL **436** is formed by PVD, CVD, electrolytic plating, or electroless plating processes. RDL **436** is deposited conformally over a surface of encapsulant **434** into the vias formed over contact pads **430** of die **428** and bumps **426**. With RDL **436** deposited, bumps **426** are electrically connected to the circuits and devices formed within die **428**.

An optional passivation layer (not shown) is deposited over the semiconductor device to cover RDL **436** and provide electrical insulation and physical protection. The optional passivation layer may include one or more layers of SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, SiON, or another insulating material.

FIG. 9 illustrates semiconductor device **500** having an interconnect structure providing top and bottom interconnects formed by solder bumps, RDLs are formed over a top surface and a bottom surface of semiconductor device **500**. Solder bumps **502** are formed using a ball drop or stencil printing process. Solder material is reflowed to form solder bumps **502**. Die **504** is mounted next to bumps **502** using die attach adhesive **508**. Die **504** includes semiconductor devices, or other electronic chips or ICs and provides various functions such as memory, controller, ASICs, processor, microcontroller, or combinations thereof. Die attach adhesive **508** includes an underfill or epoxy polymer material. Contact pads **506** are made with a conductive material, such as Al, Cu, Sn, Ni, Au, or Ag, and are electrically connected to the circuit elements formed within die **504**. Contact pads **506** are formed by PVD, CVD, electrolytic plating, or electroless plating processes, for example.

Encapsulant **510** is deposited around bumps **502** and over die **504**. Encapsulant **510** includes an epoxy resin, or polyimide, for example, and may be deposited by spin-coating, dispensing, or printing. As shown in FIG. 9, the deposition of encapsulant **510** is controlled to expose a top surface of bumps **502**. Vias are formed in encapsulant **510** by blind etching to expose contact pads **506**.

RDL **512** is deposited over encapsulant **510** to interconnect bumps **502** and contact pads **506** of die **504**. RDL **512** can be made with Ni, NiV, Cu, or other conductive materials. RDL **512** routes electrical signals between die **504** and bumps **502**. RDL **512** is formed by PVD, CVD, electrolytic plating, or electroless plating processes. With RDL **512** deposited, bumps **502** are electrically connected to the circuits and devices formed within die **504**. As shown in FIG. 9, RDL **514** is formed over a back surface of semiconductor device **500**. RDL **514** may form electrical connections between one or more bumps **502** and contact pads **506** of die **504**, or may provide an alternative electrical interconnection network for connecting semiconductor device **500** to other system components. In alternative embodiments, additional layers of under-bump metallization or polyimide layers are formed over the device to provide additional routing capability and top and bottom interconnect pad formations. Depending upon the application, RDLs **512** and **514** may be used for re-routing electrical signals and the creation of pads and/or interconnect bumps for mounting semiconductor device **500** to a PCB or for device stacking.

An optional passivation layer (not shown) is deposited over the semiconductor device to cover RDLs **512** and **514** and provide electrical insulation and physical protection. The

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optional passivation layer may include one or more layers of SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, SiON, or another insulating material.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

What is claimed:

1. A semiconductor device, comprising:
  - a semiconductor die including a contact pad disposed on a first surface of the semiconductor die;
  - an encapsulant disposed over the semiconductor die and directly contacting the first surface of the semiconductor die, the encapsulant including opposing first and second surfaces disposed as first and second outer surfaces of the semiconductor device, respectively;
  - a die attach adhesive directly contacting a second surface of the semiconductor die opposite the first surface of the semiconductor die and including a surface coplanar with the second surface of the encapsulant;
  - a plurality of bumps disposed directly in the encapsulant adjacent to the semiconductor die and including opposing first and second portions disposed at the first and second outer surfaces of the semiconductor device, respectively;
  - a via disposed in the encapsulant over the contact pad of the semiconductor die;
  - a first redistribution layer (RDL) disposed on the first surface of the encapsulant opposite the second surface of the encapsulant and electrically connected to the contact pad of the semiconductor die and the plurality of bumps; and
  - a second RDL disposed over the second surface of the encapsulant and the surface of the die attach adhesive opposite the first RDL and electrically connected to the plurality of bumps.
2. The semiconductor device of claim 1, wherein the first or second portion of the plurality of bumps is substantially coplanar with the first or second surface of the encapsulant, respectively.
3. The semiconductor device of claim 1, wherein the first or second portion of the plurality of bumps is offset with respect to the first or second surface of the encapsulant, respectively.
4. The semiconductor device of claim 1, wherein the bumps are configured in a plurality of staggered rows.
5. The semiconductor device of claim 1, further including a passivation layer formed over the first RDL or second RDL.
6. The semiconductor device of claim 1, wherein the first RDL or second RDL includes Ni, NiV, or Cu.
7. A semiconductor device, comprising:
  - a semiconductor die including a contact pad disposed on a first surface of the semiconductor die;
  - a die attach adhesive directly contacting a second surface of the semiconductor die opposite the first surface of the semiconductor die and disposed at a first outer surface of the semiconductor device;
  - an encapsulant disposed over the semiconductor die and directly contacting the first surface of the semiconductor die;
  - a bump disposed in the encapsulant adjacent to the semiconductor die and including a first portion disposed at the first outer surface of the semiconductor device and a second portion disposed at a second outer surface of the semiconductor device opposite the first outer surface;
  - a first via disposed in the encapsulant over the contact pad; and

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a first redistribution layer (RDL) disposed over the encapsulant and in the first via.

8. The semiconductor device of claim 7, further including a second via disposed in the encapsulant over a surface of the bump.
9. The semiconductor device of claim 8, wherein the second via is formed over a substantially curved surface of the bump.
10. The semiconductor device of claim 7, wherein the first RDL contacts a surface of the bump.
11. The semiconductor device of claim 7, wherein the bump includes a substantially flat surface.
12. The semiconductor device of claim 7, further including a second RDL formed over the encapsulant opposite the first RDL.
13. The semiconductor device of claim 7, wherein a surface of the bump is substantially coplanar with a second surface of the encapsulant opposite the first surface of the encapsulant.
14. The semiconductor device of claim 7, wherein a surface of the bump is offset with respect to the first surface of the encapsulant.
15. The semiconductor device of claim 7, wherein the first RDL includes Ni, NiV, or Cu.
16. A semiconductor device, comprising:
  - a semiconductor die;
  - an encapsulant disposed over the semiconductor die;
  - a bump disposed in the encapsulant and including opposing first and second portions disposed at opposing first and second outer surfaces of the semiconductor device, respectively; and
  - a first redistribution layer (RDL) disposed over the encapsulant and directly contacting the first portion of the bump at the first outer surface of the semiconductor device.
17. The semiconductor device of claim 16, further including a via disposed in the encapsulant over the bump.
18. The semiconductor device of claim 16, wherein a surface of the bump is disposed above a surface of the encapsulant.
19. The semiconductor device of claim 16, wherein a surface of the bump is substantially coplanar with a surface of the encapsulant.
20. The semiconductor device of claim 16, wherein approximately 1% to approximately 25% of the bump is disposed above the encapsulant.
21. The semiconductor device of claim 16, wherein the first RDL includes Ni, NiV, or Cu.
22. The semiconductor device of claim 16, further including a via formed in the encapsulant over the semiconductor die.
23. The semiconductor device of claim 16, further including a second RDL formed over the encapsulant opposite the first RDL.
24. The semiconductor device of claim 16, wherein a surface of the bump is substantially planar.
25. A semiconductor device, comprising:
  - a semiconductor die including a contact pad formed over a first surface of the semiconductor die;
  - an encapsulant disposed over the semiconductor die and including opposing first and second surfaces disposed as first and second outer surfaces of the semiconductor device, respectively;
  - a plurality of bumps disposed in the encapsulant adjacent to the semiconductor die and including opposing first and second portions disposed at the first and second outer surfaces of the semiconductor device, respectively;

a via disposed in the encapsulant over the contact pad of the semiconductor die; and  
a first redistribution layer (RDL) disposed directly on the first surface of the encapsulant between the contact pad of the semiconductor die and one of the plurality of 5  
bumps.

26. The semiconductor device of claim 25, wherein the bumps are configured in a plurality of rows.

27. The semiconductor device of claim 26, wherein the bumps of each row are in a staggered configuration. 10

28. The semiconductor device of claim 25, further including a second RDL formed over the encapsulant opposite the first RDL.

29. The semiconductor device of claim 25, further including a passivation layer formed over the first RDL. 15

30. The semiconductor device of claim 29, wherein the passivation layer includes one or more layers of silicon dioxide (SiO<sub>2</sub>), silicon nitride (Si<sub>3</sub>N<sub>4</sub>), or silicon oxy-nitride (SiON).

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